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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,872	KANAMORI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-18,21-25 and 28-35* is/are rejected.

7)☒ Claim(s) *7,8,19,20,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 2-5, 8, 11, 23, 27 and 30 are objected to because of the following informalities:

Claim 2, line 10, "a minute" should be changed to --the minute--.

Claims 4 and 23, "wherein:" on line 2 should be changed to --wherein the differential input portion further includes:--; and "and" on line 8 should be changed to --wherein--.

Claim 5, line 4, "a minute" should be changed to --the minute--.

Claims 8 and 27, line 2, "the" should be changed to --a--. Further, "a minute" on line 6 of claim 2 and on line 7 of claim 27 should be changed to --the minute--.

Claim 11, "electrode for" on line 5 should be changed to --transistor for--.

Claim 30, "electrode for" on line 6 should be changed to --transistor for--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11-13, 15, 30-32 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect claim 11, the recitation "the second electrode of said first transistors and the second electrode of said second electrode" on lines 3-5 lacks antecedent basis. It appears that claim 11 should depend on claim 2, instead of claim 1. Also, "said second electrode" should be changed to "said second transistor".

With respect claim 12, the recitation "the second electrode of said first transistors and the second electrode of said second transistor" on lines 3-5 lacks antecedent basis. It appears that claim 12 should depend on claim 2, instead of claim 1.

Claim 13 is indefinite because it includes the indefiniteness of claim 12.

With respect claim 15, the recitation "said second power line and the common node to which the first electrodes of said first and second transistors are connected" on lines 3-5 lacks antecedent basis. It appears that "said second power line" should be changed to --a second power line-- and claim 15 should depend on claim 2, instead of claim 1.

With respect claim 30, the recitation "the second electrode of said first transistors and the second electrode of said second electrode" on lines 4-6 lacks antecedent basis. It appears that claim 30 should depend on claim 21, instead of claim 17. Also, "said second electrode" should be changed to "said second transistor".

With respect claim 31, the recitation "the second electrode of said first transistors and the second electrode of said second electrode" on lines 4-6 lacks antecedent basis. It appears that claim 31 should depend on claim 21, instead of claim 17.

Claim 32 is indefinite because it includes the indefiniteness of claim 31.

With respect claim 34, the recitations "said second power line and the common node to which the first electrodes of said first and second transistors are connected" on lines 4-6 lacks antecedent basis. It appears that "said second power line" should be changed to --a second power line-- and claim 34 should depend on claim 21, instead of claim 17.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 9, 10 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Branson et al. (USP 5,508,644).

With respect to claim 1, Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10), which includes: a latch unit (12, 14, 16, 18) and a differential input portion (22, 20, 26, 24), wherein a minute current (small current that transistor 26 sinks) flows through the differential input portion (see Col. 3, lines 5-6).

With respect to claim 2, Figure 1 of the Branson et al. reference shows that the differential input portion (22, 20, 26, 24) includes a first transistor (22) and a second transistor (20) each having a first electrode (the electrode connected to transistor 26 for both transistors), a second electrode (the electrode connected to transistor 18 for the first transistor 22, and the electrode connected to transistor 16 for the second transistor 20) and a control electrode (gate); the control electrodes of the first and second transistors are supplied with a differential input signal (BL, BL/); and a third transistor (26) for keeping the minute current (small current that transistor 26 sinks) to flow through the first (22) and second (20) transistors is inserted between a first power line (Vss) and a common node (the node connected transistors 22 and 20 together) to which the first electrodes of the first and second transistors are connected.

With respect to claim 3, the third transistor (26) turns off the minute current (small current that transistor 26 sinks) flowing through the first (22) and second (20) transistors upon deactivation (power off) of the differential sense amplifier circuit (10). This is because upon deactivation (power off) of the differential sense amplifier circuit (10), n-channel transistor 26 will be turned off since the gate of this transistor receives no power supply (power off). Thus, transistor 26 turns off the small current flowing through transistors 22 and 20.

With respect to claim 4, Figure 1 of the Branson et al. reference shows that a fourth transistor (24) for supplying a drive current at the time of signal determination (when signal LE is at the high level) in the differential amplifier circuit is inserted between the first power line (Vss) and the common node (the node connected transistors 22 and 20 together) to which the first electrodes of the first and second transistors are connected; and the third transistor (26) is connected in parallel with the fourth transistor (24).

With respect to claim 5, Figure 1 shows that the control electrode (gate) of the third transistor (26) is supplied with a first control signal (Vdd) for constantly supplying the minute current during the operation (power on) of the differential sense amplifier (10).

With respect to claim 6, Col. 2, lines 35-40, of the Branson et al. reference discloses that a gate width of the third transistor (26) is smaller than a gate width of the fourth transistor (24).

With respect to claim 9, Figure 1 of the Branson et al. reference shows that the latch unit (12, 14, 16, 18) includes a first inverter (14, 18) inserted between the second electrode of the first transistor (22) and a second power supply (Vdd); and a second inverter (12, 16) inserted between the second electrode of the second transistor (20) and the second power supply line (Vdd), the first and second inverters being cross-coupled to each other.

With respect to claim 10, Figure 1 of the Branson et al. reference shows that the differential sense amplifier circuit (10) is configured of MOS transistors; transistors (14 and 12) of the first (14, 18) and second (12, 16) inverters which are connected to the second power line (VDD) are each connected in parallel with an additional transistor, respectively (transistor 14 is connected in parallel with transistor 36, and transistor 12 is connected in parallel with transistor 34); and the second electrode of each of the first (22) and second (20) transistors is held at a predetermined level at other than the time of signal determination during the operation of the differential sense amplifier (e.g., when LE is at low level, p-channel transistors 36 and 34 are turned on because the gates of these transistors receive a logic low to pull the outputs of the first and second inverters to logic high (power supply Vdd level); n-channel transistors 18 and 16 receive the logic high (power supply Vdd level) at their gates so that n-channel transistors 18 and 16 are turned on and the second electrode of each of the first (22) and the second (20) transistors also having the power supply Vdd level. Therefore, the second electrode of each of the first and second transistors is held at a predetermined level (logic high) when LE is at low level during operation of the differential sense amplifier.

With respect to claim 16, the differential sense amplifier (10) in Figure 1 of the Branson et al. reference is a differential sense amplifier circuit (10) of a strong arm latch type (the differential sense amplifier in Figure 1 of the Branson et al. reference has a latch unit portion, and has the same structure as that of the applicant's invention).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (each of Figures 1-7) in view of Branson et al. (UPS 5,508,644).

Each of Figures 1-7 of the applicant's admitted prior art shows a differential sense amplifier circuit which includes: a latch unit (111, 112, 121, 122) and a differential input portion (101, 122, 130) except for a minute current is kept to flow through the differential input portion. However, Figure 1 of the Branson et al. reference discloses a differential sense amplifier circuit (10) which includes a small transistor (26) that is always on during operation of the differential sense amplifier circuit (because the gate of n-channel transistor receives a power supply Vdd signal) to thereby sinks a small current from transistors 20 and 22 for the purpose of sensing a small voltage differential across the input terminals and suitable for use in high speed applications (see line 62 of Col.1 to line 10 of Col. 2). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential amplifier in each of Figures 1-7 of the applicant's admitted prior art with the small transistor, as taught in Figure 1 of the Branson et al. reference, for the purpose of sensing a small voltage differential across the input terminals of the differential amplifiers and suitable for use in high speed applications. Note that, in each of these combinations (e.g., each of Figures 1-7 of applicant's admitted prior art and the Branson et al. reference), a minute current (small current

that the small transistor 26 sinks from transistors 101 and 102 in each of Figures 1-7 of the applicant's admitted prior art) is kept to flow through the differential input portions. Also, in each of these combinations, the differential input portion (101-102 and 130 in each of Figures 1-7 of applicant's admitted prior art, and also small transistor 26 as taught Figure 1 of the Branson et al. reference) of the differential amplifier includes: a first transistor (101) and a second transistor (102) each having a first electrode (the electrode connected to transistor 130), a second electrode (the electrode connected to transistors 112 or 122) and a control electrode (gate); the control electrodes of the first and second transistors are supplied with a differential input signal (d, dx); and a third transistor (26 as taught in Figure 1 of Branson et al.) for keeping the minute current to flow through the first (101) and second (102) transistors is inserted between a first power line (AVS) and a common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first and second transistors are connected. Further, in each of these combinations, the latch unit includes a first inverter (111-112) inserted between the second electrode of the first transistor (101) and a second power supply (AVD); and a second inverter (121-122) inserted between the second electrode of the second transistor (102) and the second power supply line (AVD), the first and second inverters being cross-coupled to each other.

With respect to claim 11, the combination of Figure 2 of applicant's admitted prior art and the Branson et al. reference as discussed above shows a fifth transistor (140) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102) for shorting the second electrodes of the first and second transistors in accordance with a second control signal (CK). Note that, the Examiner treats this claim as if it depends on claim 2.

With respect to claim 12, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference as discussed above shows a sixth transistor (150) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102), wherein the sixth transistor having a control electrode (gate) supplied with a predetermined voltage (AVD). Note that, the Examiner treats this claim as if it depends on claim 2.

With respect to claim 13, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference as discussed above meets the limitation "wherein said differential input signal is at CML level" (see the description of Figure 3 of applicant's admitted prior art on lines 5-9, page 10, of the instant specification).

With respect to claim 14, the combination of Figure 4 of applicant's admitted prior art and the Branson et al. reference as discussed above shows a seventh transistor (160) inserted between two nodes (q, qx) for retrieving a differential output signal (q, qx), the seventh transistor (160) shorting the two nodes in accordance with a third control signal (CK).

With respect to claim 15, the combination of Figure 7 of applicant's admitted prior art and the Branson et al. reference as discussed above shows an eighth transistor (170) connected between the second power supply (AVD) and the common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first (101) and second (102) transistors are connected, a control electrode (gate) of the eighth transistor (170) being supplied with a fourth control signal (CK). Note that, the Examiner treats this claim as if it depends on claim 2.

8. Claims 17, 18, 21-25 and 28-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (each of Figures 1-7) in view of Branson et al. (UPS 5,508,644) and Oklobdzija et al. (USP 6,232,810).

With respect to claim 17, each of the above combinations (each of Figures 1-7 of applicant's admitted prior art and the Branson et al. reference as discussed in section 5 above) discloses a semiconductor device having a differential amplifier circuit (each of the above combinations), and a clock source (inherently, e.g., whichever source that is used to generate the clock signal CK in each of Figures 1-7 of applicant's admitted prior art) generating a clock (CK) and supplying the generated clock (CK) to the differential amplifier circuit, wherein the differential amplifier circuit includes a latch unit and a differential input portion, wherein a minute current is kept to flow through the differential input portion (see the combination of each of Figures 1-7 of applicant's admitted prior art and the Branson et al. reference as discussed in section 5 above). While each of the above combinations fails to disclose the semiconductor device includes a latch circuit latching an output signal of the differential amplifier circuit, the Oklobdzija et al. reference discloses that an SR latch circuit connected to the output of the differential sense amplifier to latch the output of the differential sense amplifier for the well-known purpose of making a D flip-flop circuit (see Figures 1 and 3, lines 13-15 of Col. 1, and lines 11-12 of Oklobdzija et al.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential sense amplifier in each of the above combinations (each of Figures 1-7 of the applicant's admitted prior art and the Branson et al. reference) with an SR latch circuit connected at the output of the differential sense

amplifier for the purpose of making a D flip-flop circuit for use in digital systems, such as processors, digital signal processors and memories.

With respect to claim 18, each of the above combinations (each of the Figures 1-7 of applicant's admitted prior art and the Branson et al. reference, and the Oklobdzija et al. reference) meets all the limitations of this claim, e.g., the semiconductor integrated circuit device is a receiving circuit (any circuitry that receives an input signal can be construed as a receiving circuit) of a signal transmission system (e.g., digital systems such as processors or memories that the differential D Flip-flop used in), the signal transmission system including a transmission circuit (inherently, e.g., whichever circuit that is used to generate the differential signal d and dx for inputting to the differential sense amplifier) outputting the differential signal, a signal transmission path (the wires connected between the output of the circuit that is used to generated differential signal d and dx to the input of the differential sense amplifier), and the receiving circuit receiving the differential signal through the signal transmission path (the wires).

With respect to claim 21, each of these combinations shows that the differential input portion (transistors 101-102 and 130 in each of Figures 1-7 of applicant's admitted prior art, and also small transistor 26 as taught Figure 1of the Branson et al. reference) of the differential amplifier includes: a first transistor (101) and a second transistor (102) each having a first electrode (the electrode connected to transistor 130), a second electrode (the electrode connected to transistors 112 or 122) and a control electrode (gate); the control electrodes of the first and second transistors being supplied with the differential input signal (d, dx); and a third transistor (26 as taught in Figure 1 of Branson et al.) for keeping the minute current to flow through the first (101) and second (102) transistors is inserted between a first power line (AVS) and a

common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first and second transistors are connected.

With respect to claim 22, in each of these combinations, the third transistor (26) turns off the minute current (small current that transistor 26 sinks) flowing through the first (101) and second (102) transistors upon deactivation (power off) of the differential sense amplifier circuit. This it because upon deactivation (power off) of the integrated circuit device, n-channel transistor 26 will be turned off since the gate of this transistor receives no power supply (power off) and thus transistor 26 turns off the small current flowing through the first and second transistors.

With respect to claim 23, each of these combinations shows that the differential input portions includes a fourth transistor (130) for supplying a drive current at the time of signal determination (when signal CK is at the high level) in the differential amplifier circuit between the first power line (AVS) and the common node (the node connected transistors 101 and 102 together) to which the first electrodes of the first and second transistors are connected; and the third transistor (26) is connected in parallel with the fourth transistor (130).

With respect to claim 24, each of the combinations (as discussed above with regard to claim 17) shows that the control electrode (gate) of the third transistor (26) is supplied with a first control signal (supply voltage signal) for constantly supplying the minute current during the operation (power on, transistor 26 always on) of the differential sense amplifier.

With respect to claim 25, each of the combinations (as discussed above with regard to claim 17) meets the limitation that a gate width of the third transistor (26) is smaller than a gate width of the fourth transistor (130).

With respect to claim 28, each of the combinations (as discussed above with regard to claim 17) shows that the latch unit includes a first inverter (111-112) inserted between the second electrode of the first transistor (101) and a second power supply (AVD); and a second inverter (121-122) inserted between the second electrode of the second transistor (102) and the second power supply line (AVD), the first and second inverters being cross-coupled to each other.

With respect to claim 29, each of the combinations (as discussed above with regard to claim 17) shows that the differential sense amplifier circuit is configured of MOS transistors; transistors (111 and 121) of the first (111, 112) and second (121, 122) inverters which are connected to the second power line (AVD) are each connected in parallel with an additional transistor, respectively (transistor 111 is connected in parallel with transistor 110, and transistor 121 is connected in parallel with transistor 120); and the second electrode of each of the first (101) and second (102) transistors is held at a predetermined level at other than the time of signal determination during the operation of the differential sense amplifier (e.g., when signal CK is at low level, p-channel transistors 110 and 120 are turned on because the gates of these transistors receive the low level so that both nodes q and qx have the same potential as the supply potential AVD, which turns on n-channels transistors 112 and 122 so the second electrode of each of the first (101) and the second (102) also having the supply potential AVD. Therefore, the second electrode of each of the first and second transistors is held at a predetermined level (supply voltage AVD) when signal CK is at low level during operation of the differential sense amplifier).

With respect to claim 30, the combination of Figure 2 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows a fifth transistor (140) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102) for shorting the second electrodes of the first and second transistors in accordance with a second control signal (CK). Note that, the Examiner treats this claim as if it depends on claim 21.

With respect to claim 31, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows a sixth transistor (150) connected to the second electrode of the first transistor (101) and the second electrode of the second transistor (102) having a control electrode (gate) supplied with a predetermined voltage (AVD). Note that, the Examiner treats this claim as if it depends on claim 21.

With respect to claim 32, the combination of Figure 3 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, meets the limitation "wherein said differential input signal is at CML level" (see the description of Figure 3 of applicant's admitted prior art on lines 5-9, page 10, of the instant specification).

With respect to claim 33, the combination of Figure 4 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows a seventh transistor (160) inserted between two nodes (q, qx) for retrieving a differential output signal (q, qx), the seventh transistor (160) shorting the two nodes in accordance with a third control signal (CK).

With respect to claim 34, the combination of Figure 7 of applicant's admitted prior art and the Branson et al. reference and the Oklobdzija et al. reference, as discussed above, shows an eighth transistor (170) connected between a second power supply (AVD) and the common node (the node connecting transistors 101 and 102 together) to which the first electrodes of the first (101) and second (102) transistors are connected, a control electrode (gate) of the eighth transistor (170) being supplied with a fourth control signal (CK). Note that, the Examiner treats this claim as if it depends on claim 21.

With respect to claim 35, in each of the combinations as discussed above with regard to claim 17, the differential sense amplifier is a differential sense amplifier circuit of a strong arm latch type.

Allowable Subject Matter

9. Claims 7, 8, 19, 20, 26 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 would be allowed because the prior art of record does not disclose or suggest all the limitations of this claim. In particular, the prior art of record fails to disclose or suggest that the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by the differential amplifier circuit (see Figures 11A-11B).

Claim 8 would be allowed because it depends on claim 7.

Claim 19 would be allowed because the prior art of record does not disclose or suggest all the limitations of this claim. In particular, the prior art of record fails to disclose or suggest an

equalizer circuit having an input connected to the differential signal and an output connected to the differential amplifier circuit (see Figure 19).

Claim 20 would be allowed because it depends on claim 19.

Claim 26 would be allowed because the prior art of record does not disclose or suggest all the limitations of this claim. In particular, the prior art of record fails to disclose or suggest that the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by the differential amplifier circuit (see Figures 11A-11B).

Claim 27 would be allowed because it depends on claim 26.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9318. The After Final fax number is (703) 872-9319.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

September 9, 2002

Long Nguyen
Art Unit: 2816